REMARKS

The Office Action dated July 9, 2004 has been received and carefully noted. The following remarks are submitted as a full and complete response thereto.

Claims 1-47 having previously been cancelled, claims 48-90 are pending in the present application. Claims 48, 56, 58, 66, 73, 75, 81-82, and 86 are independent claims. Claims 56, 63, 67-72, 78, and 88-90 have been amended exclusively for the purpose of clarity and have not been amended in view of any prior art. No new matter has been added. Claims 66, 73-77, and 79-80 having been allowed, claims 48-65, 67-72, 78, and 81-90 are respectfully submitted for consideration.

Rejection of Claims 48-65, 67-72, 78, 81-85, and 88-90 Under 35 U.S.C. § 112, Second Paragraph:

Claims 48-65, 67-72, 78, 81-85, and 88-90 were rejected under 35 U.S.C. § 112, second paragraph, as being indefinite. The above amendments to claims 67-72, 78, and 88-90 directly address the comments included in the Office Action related to these claims and render the rejection of these claims under 35 U.S.C. § 112, second paragraph, moot. However, the rejection of claims 48-65 and 81-85 is respectfully traversed.

Claim 48, upon which claims 49-55 depend, recites a wide input range amplifier that includes a first stage having first and second inputs, first and second outputs, and first, second and third voltage sources, outputting a first output signal being amplified a first amount. The wide input range amplifier also includes a second stage having first

and second inputs connected to the first and second outputs of the first stage, respectively, the second stage accepting input signals and outputting a second output signal being amplified a second amount. The first stage includes two input stages, the two input stages including a first input stage of a first conductive type and a second input stage of a second conductive type.

Claim 56, upon which claims 57 and 61-62 depend, recites a wide input range amplifier that includes a first stage having first and second inputs, first and second outputs, and first, second and third voltage sources, outputting a first output signal being amplified a first amount and a second stage having first and second inputs connected to the first and second outputs of the first stage, respectively, the second stage accepting input signals and outputting a second output signal being amplified a second amount. The first stage includes a P-type common source pair connected to a first current source and an N-type common source pair connected to a second current source, and first and second differential resistors. Also, the first current source is connected to the first voltage source, the second current source is connected to the second voltage source, a gate of a first transistor of the P-type common source pair being connected to the first input, a gate of a second transistor of the P-type common source pair being connected to the second input, a gate of a first transistor of the N-type common source pair being connected to the first input, a gate of a second transistor of the N-type common source pair being connected to the second input, a drain of the first transistor of the P-type common source pair being connected to the first output, a drain of the second transistor of the P-type

common source pair being connected to the second output, a drain of the first transistor of the N-type common source pair being connected to the first output, a drain of the second transistor of the N-type common source pair being connected to the second input, and the pair of load resistors being connected to each other and to the first and second outputs, and the mid-point of the pair of load resistors being connected to the third voltage source.

Claim 58, upon which claims 59-60 and 63-65 depend, recites a wide input range amplifier that includes a first stage having first and second inputs, first and second outputs, and first, second and third voltage sources, and outputting a first output signal being amplified a first amount. The wide input range amplifier also includes a second stage having first and second inputs connected to the first and second outputs of the first stage, respectively, the second stage accepting input signals and outputting a second output signal being amplified a second amount. The first stage further includes complementary first and second input pairs, first and second differential resistors, and a first and second pair of cascoded transistors. Also, the first input pair is of a first semi-conductor type and the second input pair is of a second semi-conductor type, and the load resistors are loaded across the first and second outputs as load resistors.

As shown above, claims 48-65 each recite wide input range amplifiers that include a first stage having "first, second, and third voltage sources". These claims were rejected because it was alleged in the Office Action that the figures of the present application only appear to illustrate two voltage sources in the first stage of the amplifiers illustrated therein. Applicants respectfully disagree at least for the reasons discussed below.

Figure 1 of the present application illustrates a representative embodiment of an amplifier recited in claims 48-65. The two stages of the amplifier illustrated in Figure 1 are pre-amplifier stage 10 and Current Mode Logic (CML) stage 20. In pre-amplifier stage 10, first source voltage VDD1, second source voltage VDD2, and common mode voltage source Vcm are illustrated. Since these elements, according to certain embodiments of the claimed invention, correspond to the "first, second, and third voltage sources" recited in claims 48-65, the figures of the present application properly illustrate all of the elements of the claimed invention.

Claims 81-85 each recite "thick device signals" and "thin device signals". These claims were rejected because it was alleged in the Office Action that only the devices, and not the signals, could be characterized as "thick" or "thin". However, Applicants respectfully submit that one of skill in the art, when practicing the claimed invention, will understand that a "thick device signal" is a signal that is associated with a "thick device" and that a "thin device signal" is a signal associated with a "thin device". In other words, "thick" and "thin", as recited in claims 81-85, properly refers to the size of the device, not of a signal.

At least in view of the above remarks, reconsideration and withdrawal of the rejection of claims 48-65 and 81-85 under 35 U.S.C. § 112, second paragraph, as being indefinite is respectfully requested.

Rejection of Claims 86 and 87 Under 35 U.S.C. § 102(b):

Claims 86 and 87 were rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,734,297 to Huijsing et al. (Huijsing '297). This rejection is respectfully traversed.

Claim 86, upon which claim 87 depends, recites a wide input range amplifier that includes a first amplifying means for accepting input signals and outputting a first output signal being amplified a first amount. The wider range amplifier also includes a second amplifying means for accepting input signals and outputting a second output signal being amplified a second amount. The first amplifying means includes a first input stage of a first conductive type and a second input stage of a second conductive type.

As discussed in the present specification, certain embodiments of the claimed invention provide a Low-Voltage Differential Signaling (LVDS) input buffer with wide common-mode input range, low duty cycle distortion, and low power consumption. It is respectfully submitted that Huijsing '297 fails to disclose or suggest the elements of any of the presently pending claims. Therefore, Huijsing '297 fails to provide at least the advantages of the claimed invention discussed above.

Huijsing '297 discloses rail-to-rail input stages with constant transconductance (g_m) and constant common-mode output currents. Huijsing '297, in Figures 5a and 5b thereof, also dislcoses bipolar embodiments of circuits that include an input stage of an operational amplifier and a control circuit.

However, Huijsing '297 fails to disclose or suggest at least that "said first amplifying means includes a first input stage of a first conductive type and a second input stage of a second conductive type", as recited in claims 86 and 87 of the present application.

In the Office Action, it is alleged that, in Figure 5b of Huijsing '297, Q1-Q4 represent complementary input pairs that are analogous to the first and second input stages of the first amplifying means recited in claims 86 and 87 of the present application. It is also alleged that elements Q11-Q14 represent cascade transistors that are analogous to the second amplifying means recited in claims 86-87.

In response to these allegations, Applicants respectfully point out that elements Q1-Q4 and Q11-Q14 are disclosed in Huijsing '297 as being either NPN or PNP switches. In other words, elements Q1-Q4 and Q11-Q14 are each disclosed as being of a first conductive type (e.g., N) and of a second conductive type (e.g., P). Therefore, elements Q1-Q4 and Q11-Q14 are not of either a "first conductive type" or of a "second conductive type", as are each of the input stages recited in claims 86-87. At least for this reason, elements Q1-Q4 and Q11-Q14 are not analogous to the first and second amplifying means recited in claims 86-87. Further, since Huijsing '297 discloses or suggests no other components that are analogous to the first and second amplifying means of the claimed invention, Huijsing '297 fails to disclose or suggest the claimed invention.

At least in view of the above remarks, reconsideration and withdrawal of the rejection of claims 86-87 under 35 U.S.C. § 102(b) as being anticipated by Huijsing '297 is respectfully requested.

Allowable Subject Matter:

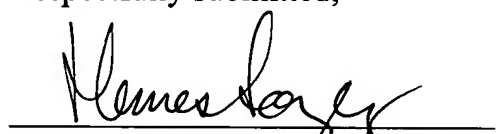
Applicants thank the Examiner for allowing claims 66, 73-77, and 79-80.

Applicants respectfully submit that all of the comments included in the Office Action have been addressed and that all of the rejections included in the Office Action have been overcome. Hence, Applicants respectfully further submit that, at least in view of the above, claims 48-90 of the present application contain allowable subject matter. Therefore, it is respectfully requested that all claims pending in the present application be allowed, and that this application be passed to issue.

If for any reason the Examiner determines that the application is not now in condition for allowance, it is respectfully requested that the Examiner contact, by telephone, the Applicants' undersigned representative at the indicated telephone number to arrange for an interview to expedite the disposition of this application.

In the event this paper is not being timely filed, the Applicants respectfully petition for an appropriate extension of time. Any fees for such an extension together with any additional fees may be charged to Counsel's Deposit Account 50-2222.

Respectfully submitted,



Hermes M. Soyez, Ph.D.
Registration No. 45,852

Customer No. 32294
SQUIRE, SANDERS & DEMPSEY LLP
14TH Floor
8000 Towers Crescent Drive
Tysons Corner, Virginia 22182-2700
Telephone: 703-720-7800
Fax: 703-720-7802
HMS:jd